

ABSTRACT

In an LSI system using an on-chip bus, when a transfer on the bus is delayed due to a fully loaded buffer in a destination module, a source module cannot proceed to the next processing. Such an unwanted situation is eliminated by a transferring buffer which is provided on a transfer path in an on-chip bus on the LSI for temporarily storing transfer data. With this transferring buffer, even if a buffer within a slave module, specified as the destination, is fully loaded and cannot accept any more transfer, a bus master can transfer data to the transferring buffer provided on the on-chip bus. Thus, the bus master is not kept waiting for execution of a transfer, irrespective of the state of the buffer within the slave, thereby improving the processing performance of the entire system.

T03077 0049260